

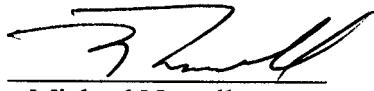
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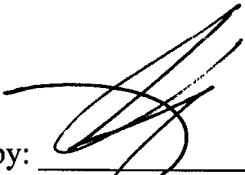
Non-Volatile Mass Memory Functional Requirements

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Non-Volatile Mass Memory Functional Requirements

Prepared by: 
Michael Newell

Approved by: 
Karl Strauss

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1 Purpose and Scope

1.1 Purpose

This document specifies requirements for the development of a Non-Volatile Mass Memory.

For the purposes of the document the term Mass Memory is defined as either a component level device (element) or a fully integrated Subassembly.

1.2 Scope

Developments controlled by this document consist of either a memory element of sufficient density, packaging, power, and configuration so as to achieve a memory Subassembly specified in Sections 6 thru 10 of this document, or of a Non-Volatile Mass Memory Subassembly which consists of a series of compliant Elements packaged and architected to achieve the requirements of Sections 6 thru 10 of this document.

1.3 Description

The Non-Volatile Mass Memory Subassembly contains electronics that allow for access to a partitionable mass memory storage array of sufficient initial capacity so as to guarantee 640Gbits (uncompressed) available memory at end of mission.

A non-volatile memory Element will have sufficient density, packaging, power, and configuration so as to achieve a compliant memory Subassembly.

1.4 Applicability

This document is applicable to all procurements of identical product.

2 Applicable Documents

The following documents are applicable:

2.1 Project Documents

JPL 982-00025, "Draft JIMO Part Program Requirements"
JPL 982-00037, "Draft JIMO Reliability Assurance Requirements"

2.2 JPL Documents

2.3 NASA/Military Documents

2.4 Industry Standards & Documents

JEP122-B - "Failure Mechanisms and Models for Semiconductor Devices"
JESD91-A - "Method for Development of Acceleration Models for
Electronic Components and Failure Mechanisms"
PICMG2.0 R3.0, CompactPCI® Specification, October 1, 1999

2.5 Order of Precedence

In case of conflict, the following order of precedence applies:

1. Contract Requirements
2. Technical Direction Memorandum
3. JPL Standards & Requirements
4. Functional Requirements
5. Contractor developed Specification
6. Industry Standards & Requirements
7. Commercial Specifications

3 REFERENCE DOCUMENT

The following is included for reference purposes.

3.1 Project Documents

JPL 982-00029 Draft JIMO Environmental Requirements Document,
dated 1/12/2004

4 Index of Abbreviations and Terms

4.1 Non-Volatility

Non-Volatility is that which is retained in memory by a means such that the removal of power does not alter or delete stored data.

4.2 KByte

A kiloByte is 8192 individual bits.

4.3 Mbit

A Megabit is 1,048,576 individual bits.

4.4 Gbit

A Gigabit is 1,073,741,824 individual bits.

4.5 Bit Error Rate

Bit Error Rate (BER) is defined as the total number of detected errors experienced per unit time.

4.6 Radiation Hardened

Radiation Hardened devices are ones that experience no degradation whatsoever below a specified Total Dose and Energetic Particle environment – usually to some extreme value.

4.7 Capacity

It is important to note that throughout this document, data storage figures represent the minimums required for data storage only and do not take into account:

- additional memory elements required for an implementation of device-internal error detection and correction (EDAC)
- additional memory elements or devices required to achieve EOM capacity requirements.

Additional memory elements required due to the above reasons are *over and above* any capacity requirement mentioned elsewhere in this document.

Capacity requirements are raw data bits.

4.8 [Bracketed Number]

Throughout this document, certain numbers appear inside brackets “[n]”. The bracketing of a number indicates that the number, while considered reasonable and proper, is subject to review and change.

5 Configuration Requirements

A Non-Volatile Mass Memory Subassembly, or the Elements therein, shall be fabricated in three distinct hardware phases. The definitions of the three phases are as follows.

5.1 Elements

5.1.1 Phase 1 – “Proof of Concept”

An Element produced for a Phase 1 development has the same device rules, processing and speed as an Element proposed for phase 2, but not necessarily the same capacity or packaging.

A Phase 1 Element will not be subjected to environmental operating requirements outside of room ambient conditions.

Phase 1 Elements shall be subject to radiation testing by the Contractor to determine compliance to the radiation requirements specified in §8.3.

Phase 1 Elements shall be marked with a C - NNN designator, where NNN is a number from 001 to the maximum number of Phase 1 Elements manufactured.

5.1.2 Phase 2 – “Required Density”

A Phase 2 Element is one which complies with all Element requirements in sections 6, 7, and 8.

Phase 2 Elements shall be subject to radiation testing by the Contractor to determine compliance to the radiation requirements specified in §8.3.

Phase 2 Elements delivered shall be marked with a B - NNN quality Designator. Where NNN is a number from 001 to the maximum number of Phase 2 Elements manufactured.

5.1.3 Phase 3 – “Flight Qualifiable Product”

A Phase 3 Element is one that complies with all Element requirements in sections 6 thru 10.

Additionally, Phase 3 Elements shall be tested to requirements of JPL 982-00025.

Phase 3 Elements shall be subject to radiation testing by the Contractor to determine compliance to the radiation requirements specified in §8.3.

Phase 3 Elements delivered shall be marked with an A -NNN quality Designator, where NNN is a number from 001 to the maximum number of Phase 3 Elements manufactured.

5.2 Subassemblies

5.2.1 Phase 1 – “Proof of Concept”

A Subassembly produced for a Phase 1 development consists of microelectronics and Elements containing the same device rules, processing and speed as the Subassembly proposed for phase 2, but not necessarily the same capacity or packaging.

A Phase 1 Subassembly is one which complies with the requirements of §6, except for the packaging requirements state in §10.

A Phase 1 Subassembly will not be subjected to environmental operating requirements outside of room ambient conditions.

Phase 1 Subassemblies shall be subject to radiation testing by the Contractor to determine compliance to the radiation requirements specified in §8.3.

Phase 1 Subassemblies shall be marked with a C - NNN designator, where NNN is a number from 001 to the maximum number of Phase 1 Subassemblies manufactured.

5.2.2 Phase 2 – “Required Density”

A Phase 2 Subassembly is one which complies with all Subassembly requirements in sections 6 thru 10.

Phase 2 Subassemblies shall be subject to radiation testing by the Contractor to determine compliance to the radiation requirements specified in §8.3.

Phase 2 Subassemblies delivered shall be marked with a B - NNN quality Designator, where NNN is a number from 001 to the maximum number of Phase 2 Subassemblies manufactured.

5.2.3 Phase 3 – “Flight Qualifiable Product”

A Phase 3 Subassembly is one that complies with all Subassembly requirements in sections 6 thru 10.

Additionally, Phase 3 Subassemblies shall be tested to requirements of JPL 982-00025.

Phase 3 Subassemblies shall be subject to radiation testing by the Contractor to determine compliance to the radiation requirements specified in §8.3.

Phase 3 Subassemblies delivered shall be marked with an A -NNN quality Designator, where NNN is a number from 001 to the maximum number of Phase 3 Subassemblies manufactured.

6 Functional Requirements

The Non-Volatile Mass Memory shall contain electronics and circuitry to meet the functional requirements defined in this section.

The Non-Volatile Mass Memory shall be verified by test and analysis as required to perform within specification as stated in this section when subjected to the Environment specified in §8.

Compliance to the requirements of §7 shall be by analysis.

Compliance to the requirements of §10 shall be by test.

6.1 Overall

Compliance to this requirement shall be by test and analysis. Methods and methodology as prescribed in JESD91 and JEP122 shall be used. Operational Lifetime shall include, as a minimum, temperature and radiation effects

6.1.1 Operational Lifetime

Any Subassembly or Element therein or microelectronics or electromechanical thereof developed to this document shall operate within specification for a period of 20 years.

6.1.2 Memory Endurance

Any Subassembly or Element therein shall demonstrate endurance without fatigue for 1.5×10^{13} write cycles in the environment specified.

6.1.3 Data Retention

Devices developed to this document shall be able to successfully read data stored within for a period of no less than 15 years after being written.

6.1.3.1 Data Refresh

The use of externally operated, controlled, or initiated refresh to achieve the data retention requirement is prohibited.

Devices using internal data refresh:

1. Shall be fully accessible by the host at all times
2. Shall demonstrate compliance with the Bit Error Rates stated in §8.3.2.1 during and after the data refresh

3. Shall not see a decrease in endurance due to data refresh.

6.2 Elements

6.2.1 Power

Memory Elements developed hereunder shall be operational at a Voltage level of 3.3VDC ± 10%.

6.3 Subassembly

A Non-Volatile Mass Memory Subassembly shall contain electronics and circuitry to meet the functional requirements defined in this sub-section.

6.3.1 Operational Overview

The Non-Volatile Mass Memory Subassembly shall allow for insertion of cPCI cards for the purposes of interfacing the Memory to sources of information, communication, and control.

The Subassembly shall contain electronics and operational software therein so as to permit creation, deletion, manipulation of independent partitions.

6.3.2 Memory Volume

The volume of the Non-Volatile Mass Memory Subassembly at delivery shall be of sufficient capacity so as to guarantee 640 Gbits uncompressed usable storage at end of mission.

6.3.3 Data & Command Interfaces

The Non-Volatile Mass Memory Subassembly shall allow for insertion of seven 3.3 volt, 33 MHz (or 66MHz) backplane 3U cPCI cards for the purposes of interfacing to the memory and controller thereof. (See Figure 1)

6.3.3.1 Data Rates

The Non-Volatile Mass Memory Subassembly shall support simultaneous operation of all cPCI interfaces at the maximum cPCI data rate.

6.3.4 Memory Controller

The Non-Volatile Mass Memory Subassembly shall contain a method to control access to and partitioning of the mass memory. This shall include a file management system that allows the cPCI interfaces to access various partitions of the mass memory.

The Controller shall allow for partitioning the memory into at least 10 volumes.

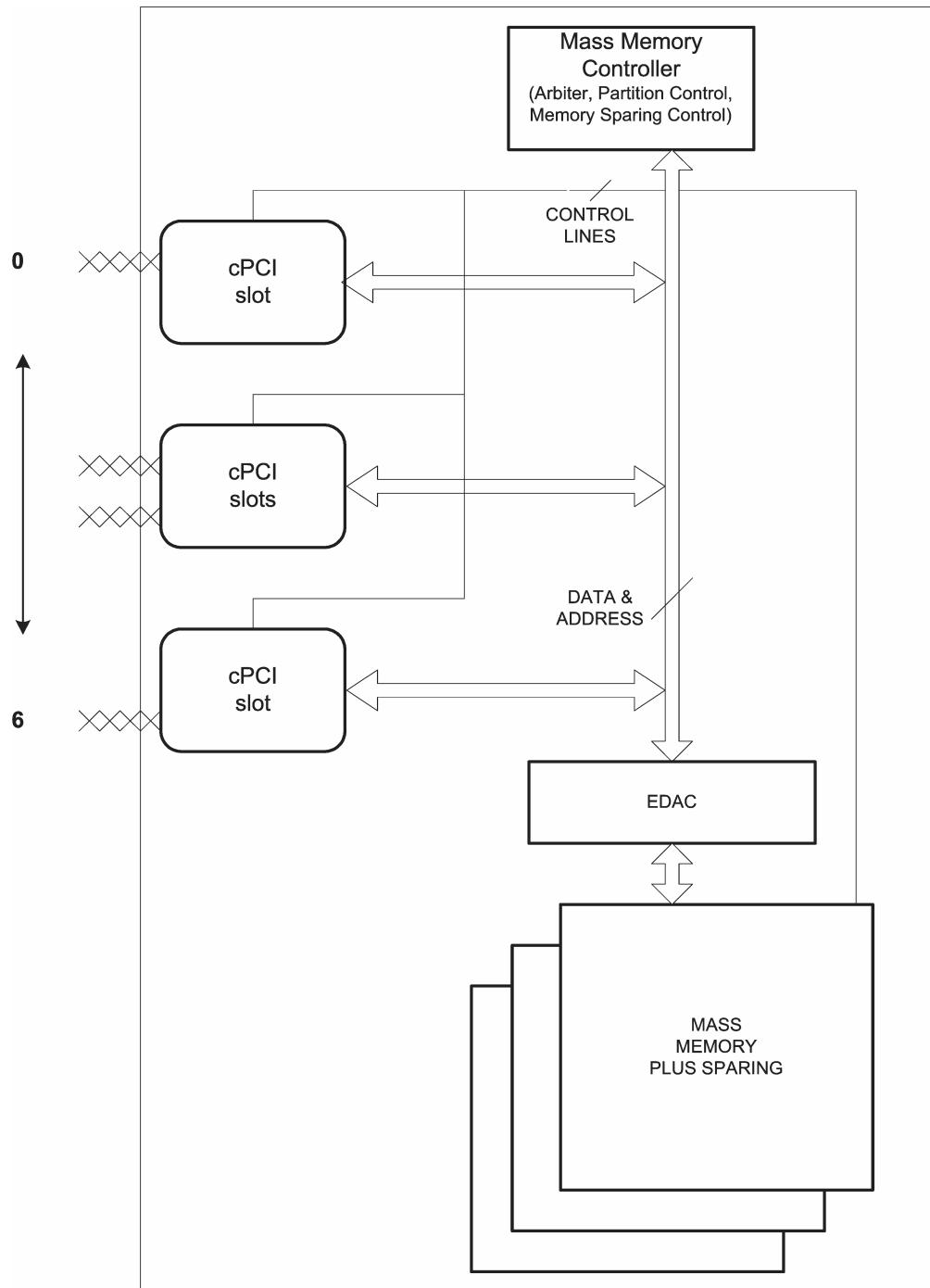


Figure 1 – Internal Functional Block Diagram for Subassembly

6.3.5 Functional Interface Definition

The Non-Volatile Mass Memory Subassembly shall be consistent with the functional signal interface shown in Figure 2.

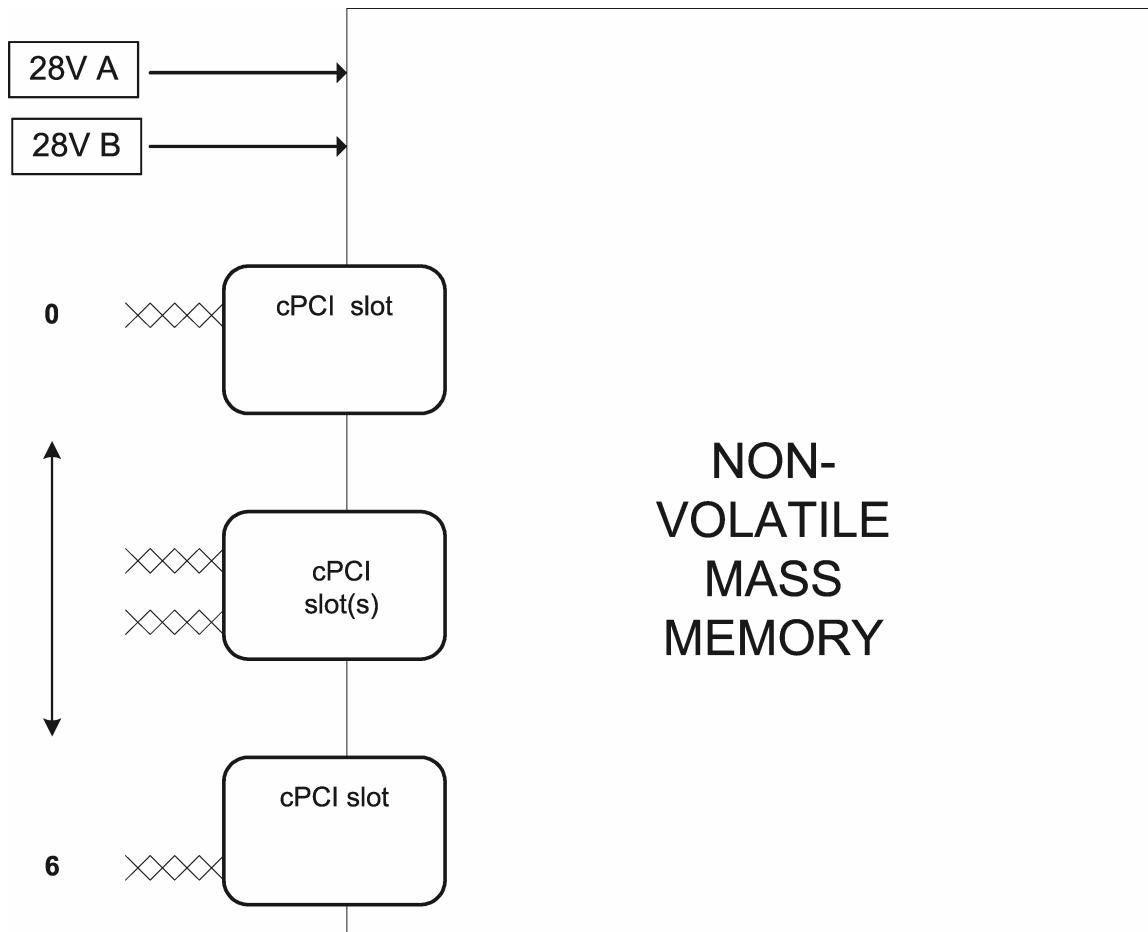


Figure 2 – Interface Functional Definition - Subassembly

6.3.6 Power

The Non-Volatile Mass Memory Subassembly (Phases 2 and 3) shall have the following power parameters :

6.3.6.1 Operating Voltage

Operating voltage: 28 VDC $\pm 10\%$.

6.3.6.2 Maximum Power - Operating

Maximum Operating Power: [50W]

6.3.6.3 Maximum Power - Standby

Maximum Standby Power: [30W]

6.3.6.4 Redundant Power Supplies (Phase 3)

The Non-Volatile Mass Memory Subassembly shall be powered by redundant power supplies. Removal of power from one power supply input shall not preclude normal operation of the Non-Volatile Mass Memory Subassembly.

7 Design Prohibitions

This section details design prohibitions.

7.1 Power Source

The Non-Volatile Mass Memory Subassembly or Element shall not rely on power stored internally for the purposes of data retention. Power shall be applied only by the external source specified in Sections 6.2.1 or 6.3.6, as applicable.

7.2 Trapped Logic States

Logical states for which there is no exit except power off are prohibited.

7.3 Data Compression

The use of data compression or other similar techniques for the purposes of delivering a Subassembly or Element with less than the required data capacity is prohibited.

8 Environmental Design Requirements

The Non-Volatile Mass Memory Subassembly or Element shall be designed to meet the environmental requirements specified below.

8.1 Requirements Applicable to All Tests at Temperature

All operational requirements as specified in §6 shall apply at any operating temperature as stated below.

8.2 Design, Analysis and Test Temperature Limits

8.2.1 Design and Analysis

8.2.1.1 Elements

The Non-Volatile Mass Memory Elements shall be designed and analyzed to meet the following temperature range: -55C to +125C.

8.2.1.2 Subassembly

The Non-Volatile Mass Memory Subassembly shall be designed and analyzed to meet the following temperatures: -40C to +85C at the thermal control surface as specified by the Contractor.

8.2.1.2.1 Subassembly Sub-elements

Microelectronic, electromechanical, and mechanical elements that form a part of a Subassembly shall be designed and analyzed to meet following temperature range: -55C to +125C.

8.2.2 Test

Phase 2 and 3 Elements and Subassemblies shall be tested for operation within specification as defined in §6 over a temperature range of -55C to +125C (Elements) or -40C to +85C (Subassembly).

Phase 3 Elements and Subassemblies shall also be tested to satisfy the requirements of JPL 982-00025.

8.2.2.1 Margin Testing

Phase 2 Elements and Subassemblies shall be subjected to margin testing requirements as specified in the procurement contract. They shall be tested for operation at a combination of low and high voltage extremes and low and high temperature extremes. Testing to parametric failure (i.e. specification non-compliance) outside of the voltage and temperature limits specified herein shall be performed.

8.3 Radiation

Devices and Subassemblies developed to this document shall show operation within specification during and after exposure to the Ionizing radiation environment specified when tested according to JPL 982-00025.

8.3.1 Radiation Total Ionizing Dose

For Elements, Subassemblies, and microelectronics & electromechanical items used in a Subassembly, a demonstration of compliance within specification following exposure to a minimum of 300 krad_(Si) TID at the die level, without shielding, is required.

Operation within specification following exposure to 1Mrad_(Si) TID at the die level, minimum, without shielding, is a goal.

8.3.2 Single Event Effects

Elements, and Subassemblies and microelectronics used with a Subassembly shall be designed, analyzed, and tested for Single Event Effects per the requirements of JPL 982-00025.

8.3.2.1 Bit Error Rate

8.3.2.1.1 Element Level

At the Element level data upset shall not exceed a rate of 1e-10 bit errors per day in the environment specified for all causes (SEE, SEFI, address error), after Element-internal EDAC, if any.

8.3.2.1.2 Subassembly Level

At the Subassembly level data upset shall not exceed [1e-6] bit errors per day errors per day in the environment specified for all causes (SEE, SEFI, address error), after EDAC, at the Interface ports.

8.3.2.2 Latch Up

The use of active circuitry to mitigate a latchup condition shall be verified by test and analysis, subject to review and acceptance by JPL.

9 Parts Quality Requirements

Notwithstanding other requirements stated herein, Elements and Subassemblies manufactured to this document for Phase 3 shall comply with the JIMO Parts Program Plan, JPL Document 982-00025.

10 Mechanical Design Requirements

10.1 Subassembly Dimensions

Phase 2 and 3 Non-Volatile Mass Memory Subassemblies shall occupy a physical volume not to exceed [0.03 m³.]

10.2 Subassembly Mass

The mass of the Subassembly shall not exceed [31kg] including all components, mounting and any radiation shielding required.

11 Non-Volatile Mass Memory Subassembly Support Equipment

The contractor shall design and deliver to JPL equipment necessary to validate the performance of the Non-Volatile Mass Memory.

12 Notes

12.1 Units of Measurement

All drawings and calculations submitted shall use the International System of Units (SI) {MKS metric system}.

12.2 Contractors and Subcontractors

Requirements specified in this document are applicable to designs and products produced by the Contractor and any subcontractor utilized therein.