

JPL D-27605

**High Speed  
Random Access Memory  
(Local Memory)  
Functional Requirements**

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# High Speed Random Access Memory (Local Memory) Requirements

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## Revision History

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## 1 Purpose and Scope

### 1.1 Purpose

This document is written to encourage development in the area of radiation tolerant/radiation hardened High Speed Random Access Memory.

### 1.2 Scope

This document defines the functional requirements for the Upgrade or Replacement of an existing 160 MByte Synchronous DRAM with high-speed radiation tolerant devices or subassemblies. For the purpose of this document, the term Unit is defined as either a package containing one or more elements, or a fully-integrated memory subassembly.

It is the goal of this development to generate a radiation hardened product that is a form, fit, and function upgrade of an existing product, thereby allowing rapid substitution without a loss in overall system performance

Options include

1. the substitution of existing SDRAM memory components with synchronous or asynchronous, volatile or nonvolatile Elements that have the same memory capacity and data transfer rates as that being substituted but with additional radiation hardness. This option is hereinafter referred to as the Memory Upgrade (Option1). Or,
2. The development of a Subassembly consisting of in-situ circuitry designed to emulate an existing SDRAM interface; an ex-situ board (slice) containing memory Elements of sufficient quantity to provide the stated capacity, as a minimum; and the means to interface the in-situ and ex-situ circuits with each other. This option is hereinafter referred to as the Replacement Subassembly (Option 2).

### 1.3 Description

The Replacement Subassembly will be a unit that contains Elements, microelectronics and circuitry necessary to allow for 160 MBytes (minimum) of memory with a compatible functional interface. The Replacement Subassembly shall be organized as 32M x 40 bits, with 32 bits of data and 8 bits for error correction code at the interface.

A Memory Upgrade would be a microelectronic device of appropriate size, power, and capacity so as to permit the viable development of a 160 MByte Replacement Subassembly as described above.

## **2 Applicable Documents**

The following documents are applicable:

### **2.1 Project Documents**

JPL 982-00025, "Draft JIMO Parts Program Requirements"  
JPL 982-00037, "Draft JIMO Reliability Assurance Requirements"

### **2.2 JPL Documents**

### **2.3 NASA/Military Documents**

### **2.4 Industry Standards & Documents**

JEP122-B - "Failure Mechanisms and Models for Semiconductor Devices"  
JESD91-A - "Method for Development of Acceleration Models for  
Electronic Components and Failure Mechanisms"  
PICMG2.0 R3.0, CompactPCI® Specification, October 1, 1999

### **2.5 Commercial Documents**

Hynix HY57V654020B 4 Bank x 4M x 4bit Synchronous DRAM data  
sheet rev. 1.7 November 2001.

### **2.6 Order of Precedence**

In case of conflict, the following order of precedence applies:

1. Contract Requirements
2. Technical Direction Memorandum
3. JPL Standards & Requirements
4. Functional Requirement
5. Contractor developed Specification
6. Industry Standards & Requirements
7. Commercial Specifications

## **3 REFERENCE DOCUMENT**

The following is included for reference purposes.

### **3.1 Project Documents**

JPL 982-00029 Draft JIMO Environmental Requirements Document

## 4 Index of Abbreviations and Terms

### 4.1 Volatility

Volatility is that which is retained in memory by a means such that the removal of power alters or deletes stored data.

### 4.2 kByte

A kiloByte is 8192 individual bits.

### 4.3 Mbit

A Megabit is 1,048,576 individual bits.

### 4.4 Word

A Word is 16 individual bits.

### 4.5 Bit Error Rate

Bit Error Rate (BER) is defined as the total number of detected errors experienced per unit time.

### 4.6 Radiation Hardened

Radiation Hardened devices are ones that experience no degradation whatsoever following exposure to a specified Total Dose and Energetic Particle environment – usually to some extreme value.

### 4.7 Capacity

It is important to note that throughout this document, data storage figures represent the minimums required for data storage only and do not take into account additional memory required for an implementation of device-internal error detection and correction (EDAC).

### 4.8 [Bracketed Number]

Throughout this document, certain numbers appear inside brackets “[n]”. The bracketing of a number indicates that the number, while considered reasonable and proper, is subject to review and change.

### 4.9 Lower case n appended to signal names

Throughout this document, certain signal names (functional signals and pin definitions) appear with a lower case “n” appended to the end of the signal name. This indicated that the signal being defined is active low true signal type. An example would be a Chip Enable signal denoted CE. CE itself would be an active high true signal (logic level ‘1’ true, whereas CEn is an active low true signal (logic level ‘0’ true).

**4.10 In-Situ**

In place locally, having direct and immediate interface with the host.

**4.11 Ex-Situ**

Not in immediate interface or contact with the host. Contained on a separate slice.

**4.12 Slice**

A euphemism for a circuit board of cPCI dimensions.

**4.13 Signal Naming (N:X)**

Shorthand for grouping together a number of signals with similar names save for the parentheticals. Example: CEn(3:0) would identify a total of four signals having the name CEn3, CEn2, CEn1, and CEn0.

## 5 Configuration Requirements

The High Speed Random Access Memory shall be fabricated in three distinct hardware phases. The definitions of the three Phases are as follows.

### **5.1 Phase 1 – “Proof of Concept”**

A unit produced for a Phase 1 development has the same device rules, processing and speed as a device proposed for Phase 2.

A Phase 1 unit is one which complies functionally with the requirements of §6, but not necessarily the same capacity or packaging.

Phase 1 units will not be subjected to environmental operating requirements outside of room ambient conditions.

Phase 1 units shall be subject to radiation testing by the contractor to determine compliance to the radiation requirements specified in §8.3.

Phase 1 units shall be marked with a C - NNN designator, where NNN is a number from 001 to the maximum number of Phase 1 units manufactured.

### **5.2 Phase 2 – “Required Density”**

A Phase 2 unit is one which complies with all requirements in sections 6, 7, 8 and 10.

Phase 2 units shall be subject to radiation testing by the contractor to determine compliance to the radiation requirements specified in §8.3.

Phase 2 units delivered shall be marked with a B - NNN quality Designator, where NNN is a number from 001 to the maximum number of Phase 2 units manufactured.

### **5.3 Phase 3 – “Flight Qualifiable”**

A Phase 3 unit is one which complies with all requirements in sections 6 thru 10.

Additionally, Phase 3 units shall be tested to requirements of JPL 982-00025.

Phase 3 units shall be subject to radiation testing by the Contractor to determine compliance to the radiation requirements specified in §8.3.

Phase 3 units delivered shall be marked with an A -NNN quality Designator, where NNN is a number from 001 to the maximum number of Phase 3 units manufactured.

## **6 Functional Requirements**

The High Speed Random Access Memory Unit shall be verified by test and analysis as required to perform within specification as stated in this section when subjected to the Environment specified in §8.

Compliance to the requirements of §7 shall be by analysis.

Compliance to the requirements of §10 shall be by test.

### **6.1 Operational Lifetime**

Compliance to this requirement shall be by test and analysis. Methods and methodology as prescribed in JESD91 and JEP122 shall be used. Operational Lifetime shall include, as a minimum, temperature and radiation effects.

#### **6.1.1 Write/Erase/Read Cycles**

Units developed to this document shall show by test and analysis no imprint or fatigue shown after  $7 \times 10^{16}$  write cycles in the specified environment.

#### **6.1.2 Device Lifetime, powered**

Units developed to this document shall operate within specification for a period of 20 years.

## **6.2 Requirements for Option 1 (Upgrade) Devices**

### **6.2.1 Memory Capacity**

Devices developed to this document for the purposes of being a Memory Upgrade shall contain, as a minimum, 256 Mbits of memory for data storage organized as 16 MWords.

### **6.2.2 Pin Electrical Characteristics**

A Memory Upgrade signal pins shall have the electrical characteristics defined in Table 1.

**Table 1 - Pin Electrical Characteristics**(T<sub>A</sub> = 25C, F = 1 MHz)

PARAMETER	CONDITIONS	SYMBOL	MIN	MAX	UNIT
Input Leakage Current	V <sub>DD</sub> = 3.6 V, V <sub>IN</sub> = 3.6 V	I <sub>LI</sub>	-5	5	µA
Output Leakage Current	V <sub>DD</sub> = 3.6 V, V <sub>OUT</sub> = 3.6 V	I <sub>LO</sub>	-5	5	µA
Input Voltage		V <sub>IL</sub> V <sub>IH</sub>	-0.3 2.0 <sup>1</sup>	0.8 V <sub>DD</sub> +0.3	V
Output Voltage	I <sub>OL</sub> = 2.0 mA I <sub>OH</sub> = -2.0 mA	V <sub>OL</sub> V <sub>OH</sub>	- 2.4	0.4 -	V
Input Capacitance		C <sub>IN</sub>	-	16	pF
I/O Capacitance		C <sub>OUT</sub>	-	6.5	pF

1. V<sub>IH</sub> min = 2.2 V for V<sub>DD</sub> = 3.6 V.

### 6.2.3 Option 1 (Upgrade) Functional Signal implementation

In basic terms, the Memory Upgrade shall be consistent with the functional signals shown in Figure 1.

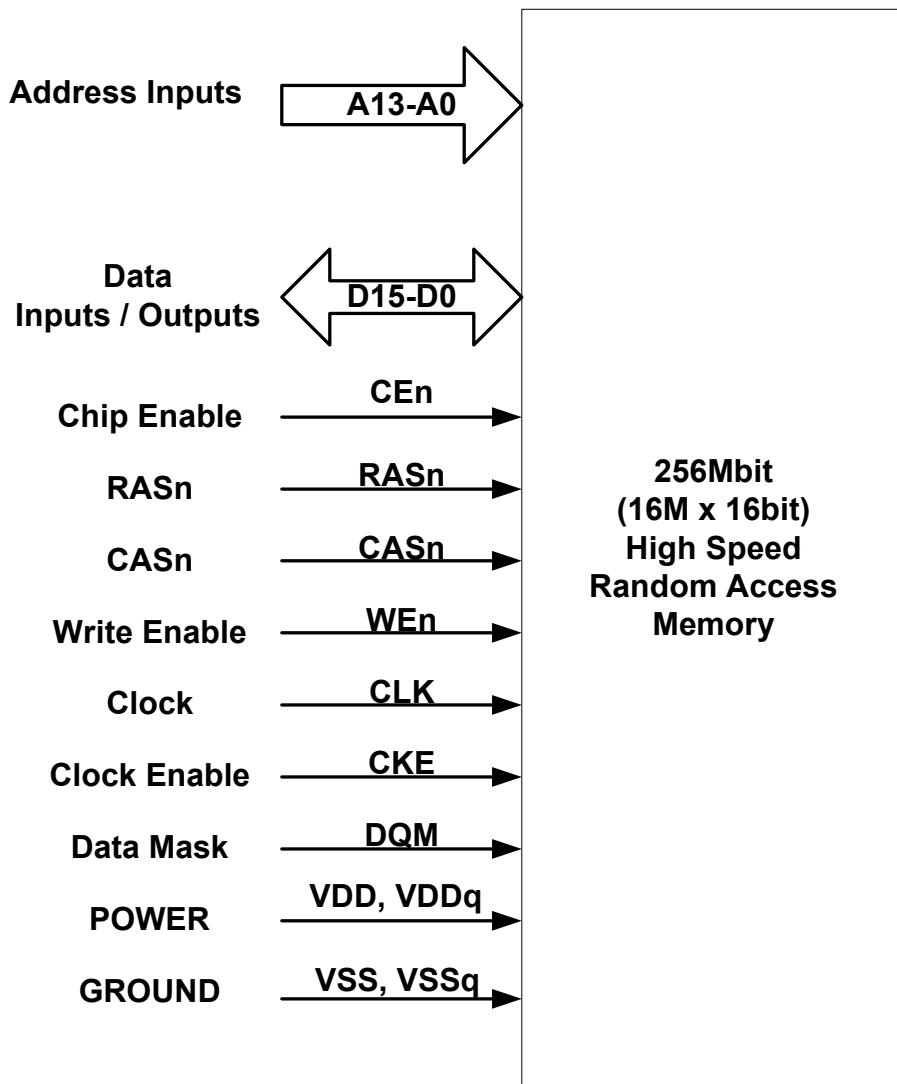


Figure 1 –Upgrade Functional Signal Implementation

### 6.2.3.1 Upgrade Function to Pin Mapping

The functional pin definitions shall map to the functional signal definition as defined in Table 2.

**Table 2 –Upgrade Signal Function to Pin Definition Map**

Functional Signal Name	Functional Pin Name
Address Inputs	A13 – A0
Data Input / Outputs	D13 – D0
Chip Enable Input	CEn
Row Address Strobe Input <sup>1</sup>	RASn
Column Address Strobe Input <sup>1</sup>	CASn
Write Enable Input	WE <sub>n</sub>
Clock	CLK
Clock Enable	CKE
Data Mask	DQM
Power Input	VDD, VDDq
Ground	VSS, VSSq

<sup>1</sup> If required.

### 6.2.3.2 Upgrade Operational Command Selection

The Memory Upgrade shall have operational modes compatible with the operational mode truth table shown in the Hynix data sheet.

### 6.2.3.3 Upgrade Mode Register Description

The Memory Upgrade shall have mode register definitions compatible with the mode register description shown in the Hynix data sheet.

### 6.2.3.4 Upgrade Timing Constraints and Waveforms

The Memory Upgrade shall support the data read, data write, data refresh and other timing waveforms and timing constraints referenced in the Hynix data sheet. The timing shall be equivalent of the specified Hynix part operating at a 100 MHz clock frequency.

## 6.2.4 Power

### 6.2.4.1 Operating Voltage, V<sub>DD</sub>

The Memory Upgrade shall be fully operational over the power input voltage range of 3.3 ± 10% volts, DC.

#### 6.2.4.2 Maximum Current

The maximum current required by a Memory Upgrade is defined as follows:

##### 6.2.4.2.1 Operating

During operation (100 MHz clock), maximum package current required by the Memory Upgrade (Phase 2 and Phase 3 parts) shall not exceed [460] mA. The current required by the Phase 1 parts shall not exceed [460] mA.

##### 6.2.4.2.2 Standby

###### 6.2.4.2.2.1 *Non Power Down Mode*

During standby, the maximum package current required by the Memory Upgrade (Phase 2 and Phase 3 parts) shall not exceed [180] mA (100 MHz clock). The current required by the Phase 1 parts shall not exceed [180] mA (100 MHz clock).

###### 6.2.4.2.2.2 *Power Down Mode*

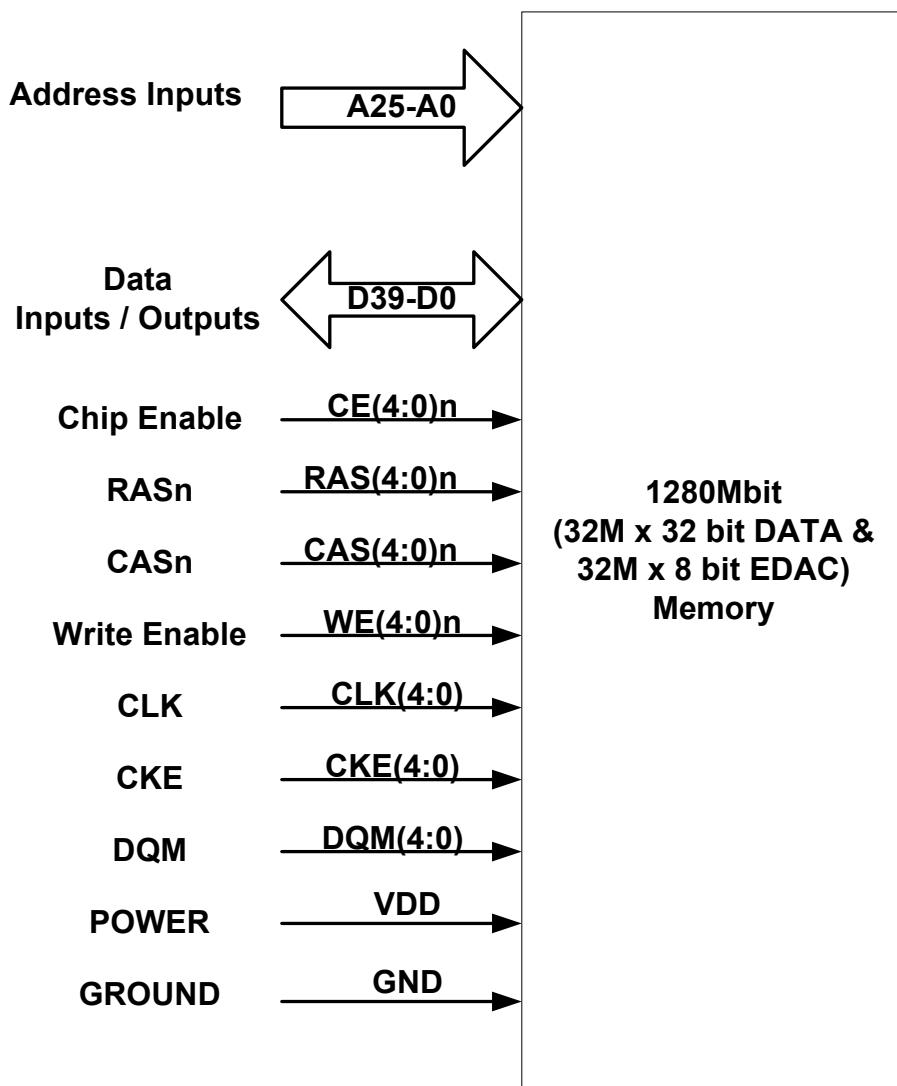
During device standby, the maximum package current required by the Memory Upgrade (Phase 2 and Phase 3 parts) shall not exceed [25] mA. The current required by the Phase 1 parts shall not exceed [25] mA.

### **6.3 Requirements for Option 2 (Replacement Subassembly) Implementation**

A Replacement Subassembly shall contain, as a minimum, 1280 Mbits of memory for data storage organized as 32 million double-words plus 8 bit EDAC (40 bit width).

#### **6.3.1 Functional Signal implementation**

In basic terms, the Replacement Subassembly shall provide the functional signal interfaces shown in Figure 2 and Table 3.



**Figure 2 – Replacement Subassembly Functional Signal Implementation**

**Table 3 - Replacement Subassembly Signal Function to Pin Definition Map**

Functional Signal Name	Functional Pin Name
Address Inputs	A25 – A0
Data Input / Outputs	D39 – D0
Chip Enable Input	CEn
Row Address Strobe Inputs <sup>1</sup>	RAS(4:0)n
Column Address Strobe Inputs <sup>1</sup>	CAS(4:0)n
Write Enable Inputs	WE(4:0)n
Clock Inputs	CLK(4:0)
Clock Enable Inputs	CKE(4:0)
Output Enable Inputs	OEn(1:0)
Data Mask	DQM(4:0)
Power Input	VDD
Ground	VSS

<sup>1</sup> If required

### 6.3.2 Functional Interface Definition

A Replacement Subassembly shall interface to the host as though it were a memory device specified in §6.2 of this document. The Replacement Subassembly implemented as an ex-situ slice, shall provide a way of emulating on-card local memory by means of qualified electronics circuitry. Interconnect between ex-situ slice and in-situ circuitry shall be by means of high speed interface supplied by the contractor. Electrical and mechanical interfacing shall be specified for review. Interface between the Replacement Subassembly and the existing host shall not use any of the existing cPCI backplane signals, except for Power, Ground, Reset, and Clock.

### 6.3.3 Pin Electrical Characteristics

The pin electrical characteristics presented by the Replacement Subassembly to the host shall be the same as specified in §6.2.2 .

### 6.3.4 Functional Interface

The interface implemented by the Replacement Subassembly shall be that as specified in §6.2.3 of this document.

### 6.3.5 Timing Constraints and Waveforms

The timing constraints for the Replacement Subassembly shall be the same constraints as described in §6.2.3.4 of this document.

### 6.3.6 Power

#### 6.3.6.1 Operating Voltage, $V_{DD}$

A Replacement Subassembly shall be fully operational over the Power Input voltage range of  $3.3 \pm 10\%$  volts, DC.

#### 6.3.6.2 Maximum Current

The maximum current required by Replacement Subassembly is defined as follows:

##### 6.3.6.2.1 Operating Current

During operation (100 MHz clock), maximum current required by the Replacement Subassembly (Phase 2 and Phase 3) shall not exceed [1600] mA. The current required by the Phase 1 Subassembly shall not exceed [1600] mA.

##### 6.3.6.2.2 Standby Current

###### 6.3.6.2.2.1 Non Power Down Mode

During standby the maximum current required by a Replacement Subassembly (Phase 2 and Phase 3) shall not exceed [900] mA (100 MHz clock). The current required by a Phase 1 Replacement Subassembly shall not exceed [900] mA (100 MHz clock).

###### 6.3.6.2.2.2 Power Down Mode

During standby, the maximum package current required by the Replacement Subassembly (Phase 2 and Phase 3) shall not exceed [175] mA (100 MHz clock). The power required by a Phase 1 Replacement Subassembly shall not exceed [175] mA (100 MHz clock).

#### 6.3.6.3 In-situ Emulation Circuitry Operating current

In addition to the current draw as specified in §6.3.6.2, the total power used to implement the in-situ local interface circuitry shall not exceed [500] mA (100MHz clock).

## **7 Design Prohibitions**

This section details design prohibitions.

### **7.1 Power Source**

Power shall be supplied only by the external source specified in §6.2.4 and §6.3.6 of this document.

### **7.2 Moving Parts**

A High Speed Random Access Memory Unit shall have no moving parts.

### **7.3 Trapped Logic States**

Logical states for which there is no exit except removal of power are prohibited.

### **7.4 Optical Interconnect**

Use of optical transmitters, receivers, and fibers are prohibited.

### **7.5 Power Sequencing**

The need to provide specific sequencing of power and any clock signals, and the initialization of any registers prior to successful operation of the device over and above that specified in the Hynix data sheet is prohibited.

## 8 Environmental Design Requirements

A High Speed Random Access Memory Unit shall be designed and tested to meet the Environmental Requirements specified below.

### 8.1 Requirements Applicable to All Tests at Temperature

All operational requirements as specified in §6 shall apply at any operating temperature as stated below.

### 8.2 Design, Analysis and Test Temperature Limits

#### 8.2.1 Design and Analysis

The High Speed Random Access Memory Units shall be designed and analyzed to be within specification at the following temperature range: -55C to +125C.

The Replacement Subassembly shall be designed and analyzed to be within specification at the following temperature range: -40C to +85C.

#### 8.2.2 Test

Phase 2 and 3 Elements and microelectronics within a Subassembly shall be tested for operation within specification as defined in §6 over a temperature range of -55C to +125C.

The Replacement Subassembly shall be tested to be within specification at the following temperature range: -40C to +85C.

Additionally, Phase 3 Units shall be tested to satisfy the requirements of JPL 982-00025.

##### 8.2.2.1 Margin Testing

Phase 2 Units subjected to margin testing requirements as specified in the procurement contract shall be tested for operation at a combination of low and high voltage extremes and low and high temperature extremes. Testing to parametric failure (i.e. specification non-compliance) outside of the voltage and temperature limits specified in sections 6.2.4.1 and 8.2.2 shall be performed.

### **8.3 Radiation**

High Speed Random Access Memory Units developed to this document shall operate within specification during and after exposure to the Ionizing Radiation environment specified when tested according to JPL 982-00025.

#### **8.3.1 Radiation Total Ionizing Dose**

A demonstration of compliance within specification following exposure to a minimum of 300 kRad<sub>(Si)</sub> TID at the die level, without shielding, is required.

Operation within specification following exposure to 1Mrad<sub>(Si)</sub> TID at the die level, minimum, without shielding, is a goal.

#### **8.3.2 Single Event Effects**

High Speed Random Access Memory Units shall be designed, analyzed, and tested for Single Event Effects per the requirements of JPL 982-00025.

##### **8.3.2.1 Bit Error Rate**

Data upset shall not exceed 1e-10 bit errors per day for all causes (SEE, SEFI, address error), measured after EDAC.

##### **8.3.2.2 Errors Spanning More Than One address**

The High Speed Random Access Memory Unit shall not exceed a rate of 6e-3 upsets/device-day for a single event induced error spanning more than one address in the specified environment.

##### **8.3.2.3 Single Event Functional Interrupts**

The High Speed Random Access Memory Unit shall not exceed a rate of 7e-5 upsets/device-day due to Single Event Functional Interrupts in the specified environment.

##### **8.3.2.4 Active Latch Up Mitigation**

The use of active circuitry to mitigate a latchup condition shall be verified by test and analysis, subject to review and acceptance by JPL .

## **9 Parts Quality Requirements**

Notwithstanding other requirements stated herein, High Speed Random Access Memory Units manufactured to this document for Phase 3 shall comply or shall contain components that comply with JPL 982-00025.

## 10 Mechanical Design Requirements

### 10.1 Option 1 (Upgrade) Packaging Requirements

#### 10.1.1 Package Dimensions

The Memory Upgrade shall be designed to meet the Mechanical Interface Requirements as defined by Figure 3 and Table 4.

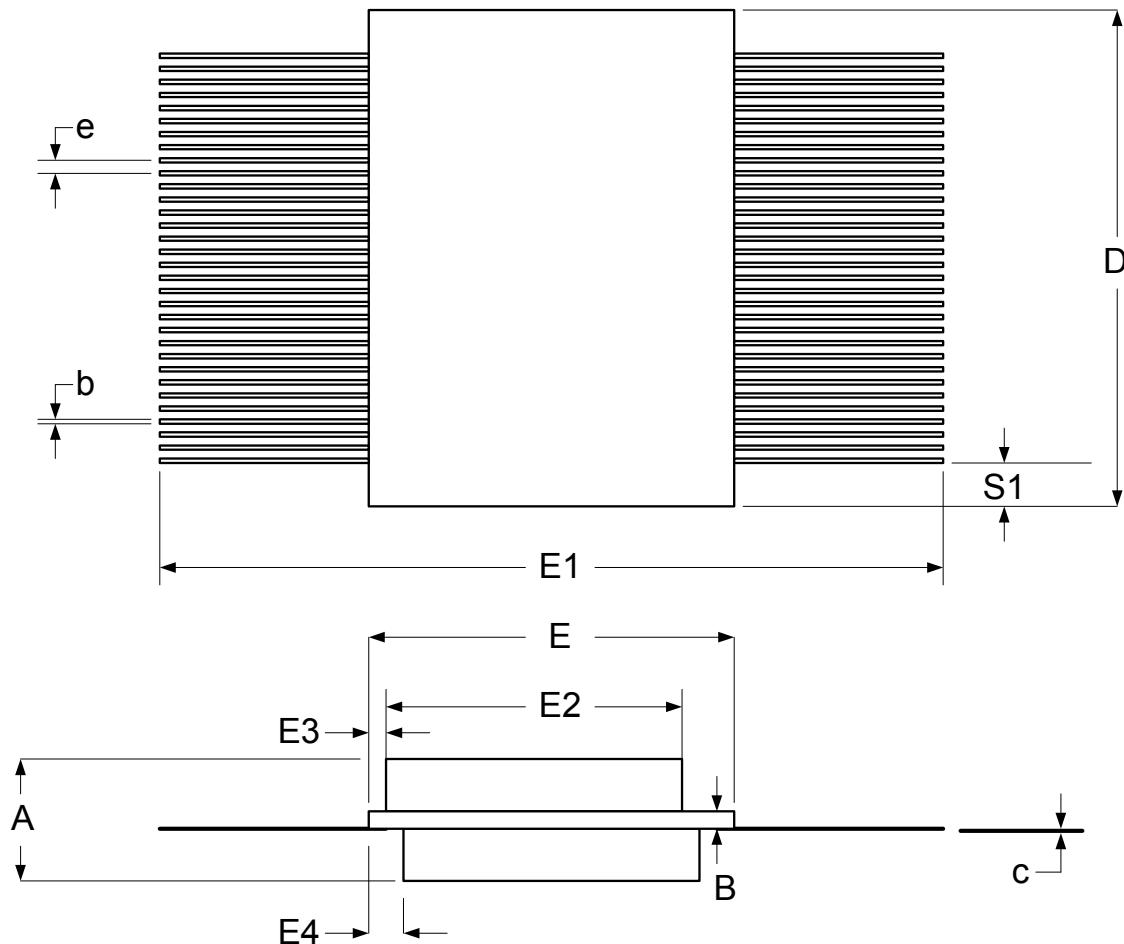


Figure 3 – Option 1 (Upgrade) Mechanical Package Diagram

**Table 4 – Option 1 (Upgrade) Mechanical Package Dimensions**

SYMBOL	DIMENSION (mm)		
	MINIMUM	NOMINAL	MAXIMUM
A	9.144	9.423	9.703
B	--	12.192	--
b	--	0.203	--
c	--	0.152	--
D	27.661	27.940	28.219
E	21.158	21.361	21.565
E1	43.282	43.866	44.450
E2	--	18.669	--
E3	--	3.708	--
E4	--	4.978	--
e	--	0.635	--
# of pins	64		

### 10.1.2 Mass

Mass of an Memory Upgrade as packaged shall not exceed 8 grams.

## **10.2 Option 2 (Replacement Subassembly) Packaging Requirements**

### **10.2.1 Volume Outline**

A Replacement Subassembly shall be designed to meet the Mechanical Package Outline Requirements as defined by Figure 4, 3U cPCI form factor. (Refer to cited cPCI specification for required dimensions.) In addition, in-situ drivers shall be packaged to meet the requirements defined in §10.1.

No more than one (1) ex-situ slice or daughter board shall be used. An ex-situ slice shall be designed to allow for its placement up to and including two cPCI slots on either side of the host.

A daughter board or ex-situ implementation shall not cause the host to exceed the 3U cPCI dimensions specified.

Due to pre-existing mechanical constraints, the use of cPCI front panel space on the host shall be kept to a minimum and is subject to review and acceptance.

### **10.2.2 Mass**

Mass of an ex-situ slice shall not exceed [330] grams including cabling. Mass of components performing the in-situ signal interface shall not exceed 8 grams.

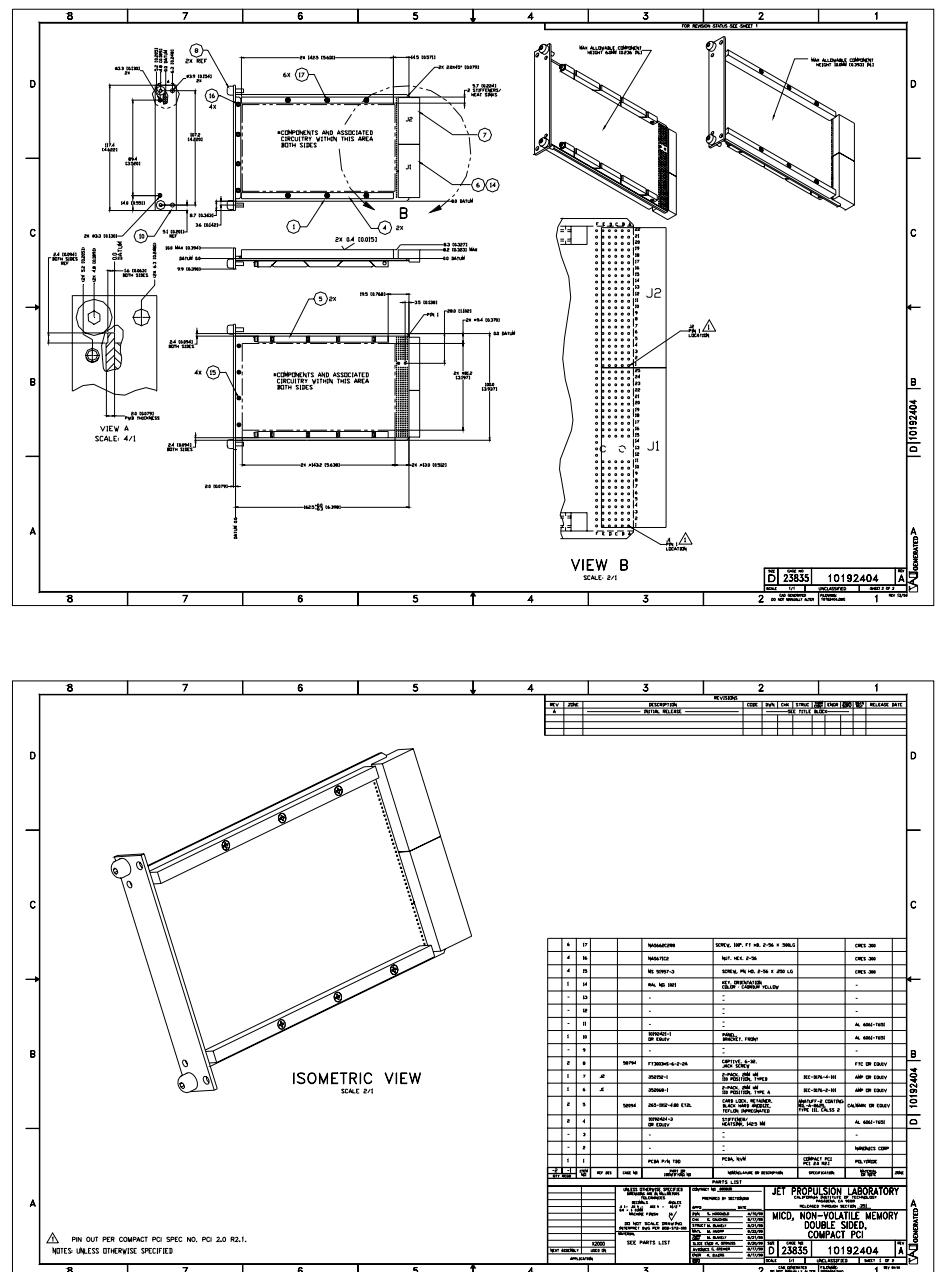


Figure 4 - Mechanical ICD cPCI slice – reference only

## **11 Replacement Subassembly Support Equipment**

If implemented as Replacement Subassembly, the contractor shall design and deliver to JPL equipment necessary to validate the performance of the Subassembly.

## **12 Notes**

### **12.1 Units of Measurement**

All drawings and calculations submitted shall use the International System of Units (SI) {MKS metric system}.

### **12.2 Contractors and Subcontractors**

Requirements specified in this document are applicable to designs and products produced by the Contractor and any subcontractor utilized therein.